ABSTRACT OF THE DISCLOSURE

A system and method avoids passive release of interrupts in a computer system. The computer system includes a plurality of processors, a plurality of input/output (I/O) devices each capable of issuing interrupts, and an I/O bridge interfacing between the I/O devices and the processors. Interrupts, such as level sensitive interrupts (LSIs), asserted by an I/O device coupled to a specific port of the I/O bridge are sent to a processor for servicing by an interrupt controller, which also sets an interrupt pending flag. Upon dispatching the respective interrupt service routine, the processor generates two ordered messages. The first ordered message is sent to the I/O device that triggered the interrupt, informing it that the interrupt has been serviced. The second ordered message directs the interrupt controller to clear the respective interrupt pending flag. Both messages are sent, in order, to the particular I/O bridge port to which the subject I/O device is coupled. After forwarding the first message to the I/O device, the bridge port forwards the second message to the interrupt controller so that the interrupt can be deasserted before the interrupt pending flag is cleared.